



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Teck Kheng Lee

Serial No.: 10/782,270

Filed: February 18, 2004

For: INTERPOSER SUBSTRATE AND
WAFFER SCALE INTERPOSER
SUBSTRATE MEMBER FOR USE WITH
FLIP-CHIP CONFIGURED
SEMICONDUCTOR DICE

Confirmation No.: 4215

Examiner: J. Clark

Group Art Unit: 2815

Attorney Docket No.: 2269-4973.1US
(00-0593.01/US)

CERTIFICATE OF MAILING

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Joseph A. Walkowski
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
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Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 or PTO/SB/08 be considered by the Examiner and made of record. Copies of U.S. patents are not being submitted pursuant to M.P.E.P. 609 III A(2). Copies of foreign patent documents and non-patent literature are enclosed pursuant to 37 C.F.R. § 1.98(a)(2).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicant herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

<u>U.S. Patent No.</u>	<u>Publication Date</u>	<u>Patentee</u>
US - 3,239,496	03/1966	Jursich
US - 4,074,342	02/1978	Honn et al.
US - 4,818,728	04/1989	Rai et al.
US - 5,148,265	09/1992	Khandros
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US - 5,489,804	02/1996	Pasch
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US - 6,177,723	01/2001	Eng et al.
US - 6,217,343	04/2001	Okuno
US - 6,222,265	04/2001	Akram et al.

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Foreign Patent Documents

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EP 0475022 A1	03/18/1992	Grube et al.
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EP 0997942 A2	05/03/2000	Horiuchi et al.
EP 1009027	06/2000	Okuno
KR 2001054744	07/2001	Choi et al. (English Abstract)

Other Documents

AL-SARAWI et al., "A review of 3-D packaging technology," *Components, Packaging, and Manufacturing Technology, Part B: IEEE Transactions on Advanced Packaging*, Vol 21, Issue 1, Feb. 1998, pp. 2-14.

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HATANAKA, H., "Packaging processes using flip chip bonder and future directions of

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- technology development," *Electronics Packaging Technology Conference*, 2002. 4th, 10-12, Dec. 2002, pp. 434-439.
- HAUG et al., "Low-Cost Direct Chip Attach: Comparison of SMD Compatible FC Soldering with Anisotropically Conductive Adhesive FC Bonding," *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 23, No. 1, Jan 2000, pp. 12-18.
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- LEE et al., "Enhancement of Moisture Sensitivity Performance of a FBGA," *Proceedings of International Symposium on Electronic Materials & Packaging*, 2000, pp. 470-475.
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- "The 2003 International Technology Roadmap for Semiconductor: Assembly and Packaging."
- TSUI et al., "Pad redistribution technology for flip chip applications," *Electronic Components and Technology Conference*, 1998. 48th IEEE, 25-28 May 1998, pp. 1098-1102.
- XIAO et al., "Reliability study and failure analysis of fine pitch solder-bumped flip chip on low-cost flexible substrate without using stiffener," *IEEE*, 2002. Proceedings 52nd, 28-31 May 2002, pp. 112-118.
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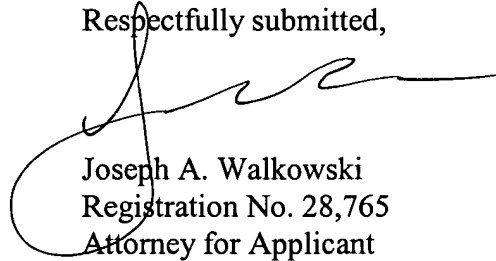
Serial No. 10/782,270

Applicant offers to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed after the mailing date of the first Office Action on the merits.

The fee pursuant to 37 C.F.R. § 1.17(p) is enclosed.

Respectfully submitted,



Joseph A. Walkowski
Registration No. 28,765
Attorney for Applicant

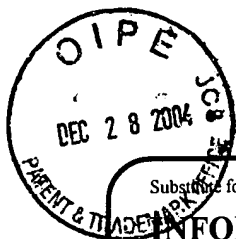
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1 of 4

Complete if Known

Application Number	10/782,270
Filing Date	February 18, 2004
First Named Inventor	Teck Kheng Lee
Group Art Unit	2815
Examiner Name	J. Clark
Attorney Docket Number	2269-4973.1US (00-0593.01/US)

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		US - 3,239,496	03/1966	Jursich	
		US - 4,074,342	02/1978	Honn et al.	
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		US - 5,148,265	09/1992	Khandros	
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		US - 6,133,637	10/2000	Hikita et al.	
		US - 6,177,723	01/2001	Eng et al.	
		US - 6,217,343	04/2001	Okuno	
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		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
		EP 0475022 A1	03/18/1992	Grube et al.		
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		KR 2001054744	07/2001	Choi et al. (English Abstract)		x

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Sheet 2 of 4

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		US - 2003/0134450 A1	07/2003	Lee	

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Teck Kheng Lee

Group Art Unit

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		AL-SARAWI et al., "A review of 3-D packaging technology," <i>Components, Packaging, and Manufacturing Technology, Part B: IEEE Transactions on Advanced Packaging</i> , Vol 21, Issue 1, Feb. 1998, pp. 2-14.	
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Sheet

4

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		LYONS et al., "A New Approach to Using Anisotropically Conductive Adhesives for Flip-Chip Assembly, Part A," <i>IEEE Transactions on Components, Packaging, and Manufacturing Technology</i> , Vol. 19, Issue 1, March 1996, pp. 5-11.	
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Invention: INTERPOSER SUBSTRATE AND WAFER SCALE
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Docket No.: 2269-4973.1US
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